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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/388,766	Applicant(s) SHIH ET AL.	
	Examiner Ayal I. Sharon	Art Unit 2123	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-35 of U.S. Application 09/388,766 filed on 09/02/1999 are presented for examination.

Claim Objections

2. Claim 6 objected to because of the following informalities: the phrase "when the released node is a preselected condition" should be "when the released node is in a preselected condition". Examiner has examined the claim interpreted the phrase according to the latter phrase. Appropriate correction is required.
3. Claim 19 appears to be an apparatus claim that is dependant upon a method claim. For the purposes of compact prosecution, Examiner has treated the claim as a method claim. Appropriate correction is required.

Claim Interpretations

4. Examiner interprets a "node" as being as being a input or output to one or more gates in a circuit. Thus, Examiner interprets that the terms "signal" and "node", are interchangeable.

5. Examiner interprets a "forced" logic value as being one of the "forcing" values defined in the definition of the "std_logic" package in IEEE Standard 1164-1993, p.2, which is held constant.
6. Applicant defines the "release" of a node as meaning that "the simulation program is free to change the logic value of the node if [the] simulation warrants a change in the logic value. Before the release, the logic value of the node is forced." (Specification, p.5)
7. Examiner interprets the "release of a node" as being equivalent to enabling a change in the logic value of the node.
8. Applicant defines "resolving" a node as meaning that "the inputs to the node are known and therefore the logic value of the node can be determined through simulation by the simulation program." (Specification, pp.5-6)
9. Examiner interprets "resolving" a node as having its value determined according to the resolution table and truth tables defined in IEEE Standard 1164-1993, pp.4-5.
10. Examiner interprets that one possible "predetermined condition" for "releasing" a node is a rising or falling edge of a clock pulse.
11. Examiner interprets "predetermined amount of time" as being the length of an entire clock cycle or a number of clock cycles.
12. Examiner interprets that a waveform plot (signal graph) is a form of "error indication" and "providing an indication when the node is in an undesirable condition", and "outputting a node condition".

13. Examiner interprets that a user-defined length of a clock cycle, or a user-defined number of clock cycles, constitutes a "user-defined time period".

14. Examiner interprets "therefrom" as being equivalent to "from this" or "from that".

15. Examiner interprets "conveyance" as being the input of a signal value.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

17. The prior art cited is as follows:

18. IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164). Copyright 1993. (Henceforth referred to as "IEEE 1164").

19. Mueller, Martin. "Chronology TimingDesigner V1.2", Printed Circuit Design, San Francisco, CA. January 1993. (Henceforth referred to as "Mueller")

20. Tzartzanis, Nestoras. "Verilog for Behavioral Modeling". February 3, 1998. Reprinted from www-scf.usc.edu/~ee577/tutorial/verilog/verilog_lec.pdf (Henceforth referred to as "Tzartzanis")

21. The claims are subsequently recited for Applicant's convenience. Applicant's attention is also directed to the pertinent sections of the prior art.

22. Claims 1-4, 6-8, 12-18, 20-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mueller.

23. Claims 25-27 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by IEEE 1164.

24. Claims 1-8, 12-30, 33-35 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tzartzanis.

25. Mueller teaches the limitations of Claim 1:

1. A method of simulating a node, comprising:
forcing an initial logic state on the node;
(Mueller, p.2, "Creating Signals")

releasing the node if a predetermined condition is met and creating therefrom a released node;
(Mueller, p.2, "Creating Signals", "Creating Clocks", and p.3 "Delays and Constraints", "Miscellaneous")

monitoring the released node; and
(Mueller, p.3, "Delays and Constraints", "Miscellaneous")

providing an indication when the released node is in a preselected condition.
(Mueller, p.3, "Miscellaneous")

26. Tzartzanis teaches the limitations of Claim 1:

1. A method of simulating a node, comprising:
forcing an initial logic state on the node;

(Tzartzanis, p.55)

releasing the node if a predetermined condition is met and creating therefrom a released node;
(Tzartzanis, p.37)

monitoring the released node; and
(Tzartzanis, pp.65-66)

providing an indication when the released node is in a preselected condition.
(Tzartzanis, pp.63-64, p.67, p.70)

27. As per Claim 2, Mueller teaches the limitations of Claim 1, as described above. Mueller also teaches the limitations of Claim 2:

2. The method of claim 1, wherein forcing the initial logic state includes forcing to a logic zero, logic one or high-impedance.
(Mueller, p.2, "Creating Signals")

28. As per Claim 2, Tzartzanis teaches the limitations of Claim 1, as described above. Tzartzanis also teaches the limitations of Claim 2:

2. The method of claim 1, wherein forcing the initial logic state includes forcing to a logic zero, logic one or high-impedance.
(Tzartzanis, p.8)

29. As per Claim 3, Mueller teaches the limitations of Claim 1, as described above. Mueller also teaches the limitations of Claim 3:

3. The method of claim 1, wherein releasing the node further comprises determining that the condition is met after passage of a predetermined amount of time.
(Mueller, p.3, "Delays and Constraints")

30. As per Claim 3, Tzartzanis teaches the limitations of Claim 1, as described above. Tzartzanis also teaches the limitations of Claim 3:

3. The method of claim 1, wherein releasing the node further comprises determining that the condition is met after passage of a predetermined amount of time.
(Tzartzanis, p.37, pp.46-50)

31. As per Claim 4, Mueller teaches the limitations of Claims 1 and 3, as described above. Mueller also teaches the limitations of Claim 4:

4. The method of claim 3, wherein releasing the node further comprises determining that the condition is met when the node has been resolved.
(Mueller, p.2 "Creating Clocks", p.3, "Delays and Constraints", "Miscellaneous")

32. As per Claim 4, Tzartzanis teaches the limitations of Claims 1 and 3, as described above. Mueller also teaches the limitations of Claim 4:

4. The method of claim 3, wherein releasing the node further comprises determining that the condition is met when the node has been resolved.
(Tzartzanis, p.37)

33. As per Claim 5, Tzartzanis teaches the limitations of Claim 1, as described above. Mueller also teaches the limitations of Claim 5:

5. The method of claim 1, wherein providing an indication includes indicating when the released node is in an unknown logic state.
(Tzartzanis, p.8)

34. As per Claim 6, Mueller teaches the limitations of Claim 1, as described above. Mueller also teaches the limitations of Claim 6:

6. The method of claim 1, further comprising providing an error indication when the released node is a preselected condition.
(Mueller, p.3, "Miscellaneous")

35. As per Claim 6, Tzartzanis teaches the limitations of Claim 1, as described above. Tzartzanis also teaches the limitations of Claim 6:

6. The method of claim 1, further comprising providing an error indication when the released node is a preselected condition.
(Tzartzanis, p.63, 67-70)

36. As per Claim 7, Mueller teaches the limitations of Claims 1 and 3, as described above. Mueller also teaches the limitations of Claim 7:

7. The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.
(Mueller, p.2, "Design Environment", and p.3 "Delays and Constraints", and p.3 "Miscellaneous")

37. As per Claim 7, Tzartzanis teaches the limitations of Claims 1 and 3, as described above. Tzartzanis also teaches the limitations of Claim 7:

7. The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.
(Tzartzanis, p.46-50)

38. Mueller teaches the limitations of Claim 8:

8. A method of initializing and monitoring a simulated circuit node, comprising:

obtaining an initial node condition for a node;
(Mueller, p.2 "Creating Signals", and p.3 "Delays and Constraints", and p.3, "Miscellaneous")

forcing the node to the initial node condition;
(Mueller, p.2 "Creating Signals")

simulating a circuit containing the node;
(Mueller, p.2 "Creating Signals", and p.3 "Delays and Constraints", and p.3, "Miscellaneous")

testing the node for a valid condition;
(Mueller, p.2 "Creating Signals", and p.3, "Miscellaneous")

monitoring the node; and
(Mueller, p.3, "Miscellaneous")

providing an indication when the node is in an undesirable condition.
(Mueller, p.3, "Miscellaneous")

39. Tzartzanis teaches the limitations of Claim 8:

8. A method of initializing and monitoring a simulated circuit node, comprising:

obtaining an initial node condition for a node;
(Tzartzanis, p.55)

forcing the node to the initial node condition;
(Tzartzanis, p.55)

simulating a circuit containing the node;
(Tzartzanis, pp.36-50)

testing the node for a valid condition;
(Tzartzanis, p.37)

monitoring the node; and
(Tzartzanis, pp.65-66)

providing an indication when the node is in an undesirable condition.
(Tzartzanis, pp.63, 67-70)

40. As per Claim 12, Mueller teaches the limitations of Claim 8, as described above. Mueller also teaches the limitations of Claim 12:

> 12. The method of claim 8, further comprising outputting the condition of the simulated node.
> (Mueller, p.3, "Miscellaneous")

41. As per Claim 12, Tzartzanis teaches the limitations of Claim 8, as described above. Tzartzanis also teaches the limitations of Claim 12:

> 12. The method of claim 8, further comprising outputting the condition of the simulated node.
> (Tzartzanis, pp.63, 67-70)

42. As per Claim 13, Mueller teaches the limitations of Claim 8, as described above. Mueller also teaches the limitations of Claim 13:

> 13. The method of claim 8, further comprising obtaining a simulation run time.
> (Mueller, p.3, "Miscellaneous")

43. As per Claim 13, Tzartzanis teaches the limitations of Claim 8, as described above. Tzartzanis also teaches the limitations of Claim 13:

> 13. The method of claim 8, further comprising obtaining a simulation run time.
> (Tzartzanis, pp.44-50)

44. As per Claim 14, Mueller teaches the limitations of Claims 8 and 13, as described above. Mueller also teaches the limitations of Claim 14:

> 14. The method of claim 13, further comprising outputting a final node condition when the simulation run time is completed.
> (Mueller, p.3, "Miscellaneous")

45. As per Claim 14, Tzartzanis teaches the limitations of Claims 8 and 13, as described above. Tzartzanis also teaches the limitations of Claim 14:

> 14. The method of claim 13, further comprising outputting a final node condition when the simulation run time is completed.
> (Tzartzanis, pp.63, 67-70)

46. Mueller teaches the limitations of Claim 15:

15. A computer-readable medium having computer-executable instructions comprising:

forcing an initial logic state on the node;
(Mueller, p.2, "Creating Signals")

releasing the node if a predetermined condition is met and creating therefrom a released node;
(Mueller, p.2, "Creating Signals", "Creating Clocks", and p.3 "Delays and Constraints")

monitoring the released node; and
(Mueller, p.3, "Delays and Constraints", "Miscellaneous")

providing an indication when the released node is in a preselected condition.
(Mueller, p.3, "Miscellaneous")

47. Tzartzanis teaches the limitations of Claim 15:

15. A computer-readable medium having computer-executable instructions comprising:

forcing an initial logic state on the node;
(Tzartzanis, p.55)

releasing the node if a predetermined condition is met and creating therefrom a released node;
(Tzartzanis, p.37)

monitoring the released node; and
(Tzartzanis, pp.65-66)

providing an indication when the released node is in a preselected condition.
(Tzartzanis, pp.63-64, p.67, p.70)

48. As per Claim 16, Mueller teaches the limitations of Claim 15, as described above.

Mueller also teaches the limitations of Claim 16:

16. The medium of claim 15, having further computer-executable instructions for forcing the initial logic state to a logic zero, logic one or high-impedance.
(Mueller, p.2, "Creating Signals")

49. As per Claim 16, Tzartzanis teaches the limitations of Claim 15, as described above. Tzartzanis also teaches the limitations of Claim 16:

16. The medium of claim 15, having further computer-executable instructions for forcing the initial logic state to a logic zero, logic one or high-impedance.
(Tzartzanis, p.8)

50. As per Claim 17, Mueller teaches the limitations of Claim 15, as described above.

Mueller also teaches the limitations of Claim 17:

17. The medium of claim 15, having further computer-executable instructions for determining that the condition is met after passage of a predetermined amount of time.
(Mueller, p.3, "Delays and Constraints")

51. As per Claim 17, Tzartzanis teaches the limitations of Claim 15, as described above. Tzartzanis also teaches the limitations of Claim 17:

17. The medium of claim 15, having further computer-executable instructions for determining that the condition is met after passage of a predetermined amount of time.
(Tzartzanis, pp.46-50)

52. As per Claim 18, Mueller teaches the limitations of Claim 15, as described above. Mueller also teaches the limitations of Claim 18:

18. The medium of claim 15, having further computer-executable instructions for determining that the condition is met when the node has been resolved
(Mueller, p.2 "Creating Clocks", p.3, "Delays and Constraints", "Miscellaneous")

53. As per Claim 18, Tzartzanis teaches the limitations of Claim 15, as described above. Tzartzanis also teaches the limitations of Claim 18:

18. The medium of claim 15, having further computer-executable instructions for determining that the condition is met when the node has been resolved
(Tzartzanis, pp.37)

54. Tzartzanis teaches the limitations of Claim 19:

19. The medium of claim 8, having further computer-executable instructions for indicating when the released node is in an unknown logic state.
(Tzartzanis, p.8, pp.63, 67-70)

55. Mueller teaches the limitations of Claim 20:

20. A simulation module for initializing and monitoring a simulated circuit node, comprising:

an input means for inputting an initial node condition;
(Mueller, p.2, "Design Environment", "Creating Signals", p.3 "Miscellaneous")

a conveying means for conveying the initial node condition to a simulated node;
(Mueller, p.2, "Design Environment", "Creating Signals", p.3 "Miscellaneous")

release means for releasing the node upon satisfaction of a condition;
(Mueller, p.2, "Design Environment", "Creating Signals", p.3 "Delays and Constraints", "Miscellaneous")

a monitoring means for monitoring the simulated node for a node condition;
(Mueller, p.3, "Miscellaneous")

and an output means for outputting an indication when the node condition is in an undesirable state.
(Mueller, p.3, "Miscellaneous")

56. Tzartzanis teaches the limitations of Claim 20:

20. A simulation module for initializing and monitoring a simulated circuit node, comprising:
an input means for inputting an initial node condition;
(Tzartzanis, p.55)

a conveying means for conveying the initial node condition to a simulated node;
(Tzartzanis, p.55)

release means for releasing the node upon satisfaction of a condition;
(Tzartzanis, p.37)

a monitoring means for monitoring the simulated node for a node condition;
(Tzartzanis, pp.65-66)

and an output means for outputting an indication when the node condition is in an undesirable state.
(Tzartzanis, pp.63-64, p.67, p.70)

57. As per Claim 21, Mueller teaches the limitations of Claim 20, as described above.

Mueller also teaches the limitations of Claim 21:

21. The module of claim 20, further comprising an output means for outputting the node condition.
(Mueller, p.3, "Miscellaneous")

58. As per Claim 21, Tzartzanis teaches the limitations of Claim 20, as described above. Tzartzanis also teaches the limitations of Claim 21:

21. The module of claim 20, further comprising an output means for outputting the node condition.
(Tzartzanis, pp.63, 67-70)

59. As per Claim 22, Mueller teaches the limitations of Claim 20, as described above.

Mueller also teaches the limitations of Claim 19:

22. The module of claim 20, further comprising an input means for inputting a

simulation run time.
(Mueller, p.2-3, "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

60. As per Claim 22, Tzartzanis teaches the limitations of Claim 20, as described above. Tzartzanis also teaches the limitations of Claim 19:

22. The module of claim 20, further comprising an input means for inputting a simulation run time.
(Tzartzanis, p.60)

61. As per Claim 23, Mueller teaches the limitations of Claim 22, as described above. Mueller also teaches the limitations of Claim 23:

23. The module of claim 22, further comprising an output means for outputting a final node condition at completion of the simulation run time.
(Tzartzanis, pp.63, 67-70)

62. As per Claim 23, Tzartzanis teaches the limitations of Claim 22, as described above. Tzartzanis also teaches the limitations of Claim 23:

23. The module of claim 22, further comprising an output means for outputting a final node condition at completion of the simulation run time.
(Mueller, p.3, "Miscellaneous")

63. Mueller teaches the limitations of Claim 24:

24. A computerized system for initializing and monitoring a simulated circuit node, the system comprising:

a circuit simulation tool;
(Mueller, p.1, Abstract, and para. 1)

a first input module inputting an initial node condition;
(Mueller, p.2, "Creating Signals")

a conveying module conveying the initial node condition to a simulated node;
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

a release module releasing the initial condition;
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

a monitoring module monitoring the simulated node for a node condition;
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

a first output module outputting an indication when the node condition is in an undesirable state;
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

a second input module inputting a simulation run time; and
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous" Note: Mueller expressly teaches "Each new signal" ... and "Printing of timing diagrams is done by specifying the range of signals and time intervals to be printed")

a second output module outputting a final node condition at completion of the simulation run time.
(Mueller, p.2-3, "Creating Signals", "Creating Clocks", p.3 "Delays and Constraints", "Miscellaneous")

64. Tzartzanis teaches the limitations of Claim 24:

24. A computerized system for initializing and monitoring a simulated circuit node, the system comprising:
a circuit simulation tool;
(Tzartzanis, p.3)

a first input module inputting an initial node condition;
(Tzartzanis, p.55)

a conveying module conveying the initial node condition to a simulated node;
(Tzartzanis, pp.59-61)

a release module releasing the initial condition;
(Tzartzanis, p.37)

a monitoring module monitoring the simulated node for a node condition;
(Tzartzanis, pp.65-66)

a first output module outputting an indication when the node condition is in an undesirable state;
(Tzartzanis, pp.63, 67-70)

a second input module inputting a simulation run time; and
(Tzartzanis, p.55 and pp.58-61)

a second output module outputting a final node condition at completion of the simulation run time.
(Tzartzanis, pp.63, 67-70)

65. IEEE 1164 teaches the limitations of Claim 25:

25. An HDL initial condition module comprising a means for maintaining a logic level of a simulated circuit node until a release condition is met.
(IEEE 1164, pp.2-5)

66. Tzartzanis teaches the limitations of Claim 25:

25. An HDL initial condition module comprising a means for maintaining a logic level of a simulated circuit node until a release condition is met.
(Tzartzanis, p.37)

67. As per Claim 26, IEEE 1164 teaches the limitations of Claim 25, as described above. IEEE 1164 also teaches the limitations of Claim 26:

26. The module of claim 25 wherein the release condition is when the node can be resolved to a known logic state.
(IEEE 1164, pp.2-5)

68. As per Claim 26, Tzartzanis teaches the limitations of Claim 25, as described above. Tzartzanis also teaches the limitations of Claim 26:

26. The module of claim 25 wherein the release condition is when the node can be resolved to a known logic state.
(Tzartzanis, p.8)

69. As per Claim 27, IEEE 1164 teaches the limitations of Claim 25, as described above. IEEE 1164 also teaches the limitations of Claim 27:

27. The module of claim 25 wherein the logic level is a value defined by an HDL executable simulation program.
(IEEE 1164, pp.2-5)

VHDL is an HDL executable simulation language.

70. As per Claim 27, Tzartzanis teaches the limitations of Claim 25, as described above. Tzartzanis also teaches the limitations of Claim 27:

27. The module of claim 25 wherein the logic level is a value defined by an HDL executable simulation program.
(Tzartzanis, pp.3, and 8)

Verilog is an HDL executable simulation language.

71. Tzartzanis teaches the limitations of Claim 28:

28. An HDL initial condition module having an initial condition release means and a simulated circuit node error detection means.
(Tzartzanis, pp.28-36, pp.65 - pp.70)

72. Tzartzanis teaches the limitations of Claim 29:

29. An HDL initial condition module comprising means for maintaining a logic level of a simulated circuit node for a predetermined period of time,
(Tzartzanis, pp.35-36, pp.46-50)

means for releasing an initial condition,
(Tzartzanis, pp.28-38)

and wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.
(Tzartzanis, pp.35-36, pp.46-50)

73. As per Claim 30, Tzartzanis teaches the limitations of Claim 29, as described above. Tzartzanis also teaches the limitations of Claim 30:

30. The module of claim 29, wherein the predetermined period of time is a user defined period of time.
(Tzartzanis, pp.35-36, pp.46-50)

74. Tzartzanis teaches the limitations of Claim 33:

33. An HDL design tool, comprising:
a circuit simulation device; and
(Tzartaris, p.3)

a plurality of selectable modules capable of being linked to the circuit simulation device,
(Tzartaris, p.51-60)

wherein at least one of the selectable modules executes the following commands:

inputting an initial node condition;
(Tzartaris, p.55)

conveying the initial node condition to a simulated node;
(Tzartaris, p.55)

releasing the node if a condition is met;
(Tzartaris, p.37)

monitoring the simulated node for a node condition; and
(Tzartaris, pp.65-66)

an output means for outputting an indication when the node condition is in an undesirable state.
(Tzartaris, p.70)

75. Tzartzanis teaches the limitations of Claim 34:

34. A simulation method, comprising:

phase one, including;

forcing an initial logic zero, logic one or high-impedance on a node;
(Tzartzanis, p.8 and p.55)

releasing the node;
(Tzartzanis, p.37)

testing to see if the node has been resolved;
(Tzartzanis, p.37)

if the node has been resolved, continue to phase two
(Tzartzanis, p.52, pp.60-61)

if the node has not been resolved, continuing in phase one
phase two, including;
(Tzartzanis, p.37)

monitoring the node value;
(Tzartzanis, pp.65-66)

testing the node value;
(Tzartzanis, p.37)

indicating an error if an unacceptable condition appears on the node;
(Tzartzanis, pp.60-67)

and, continuing in phase two until simulation completion.
(Tzartzanis, pp.58-62)

76. Tzartzanis teaches the limitations of Claim 35:

35. The method of claim 34, wherein simulation completion is a user defined time period.
(Tzartzanis, pp.46-50)

Claim Rejections - 35 USC § 103

77. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

78. The prior art cited is as follows:

79. IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164). Copyright 1993. (Henceforth referred to as "IEEE 1164").

80. Mueller, Martin. "Chronology TimingDesigner V1.2", Printed Circuit Design, San Francisco, CA. January 1993. (Henceforth referred to as "Mueller")

81. Tzartzanis, Nestoras. "Verilog for Behavioral Modeling". February 3, 1998. Reprinted from www-scf.usc.edu/~ee577/tutorial/verilog/verilog_lec.pdf (Henceforth referred to as "Tzartzanis")

82. The claims are subsequently recited for Applicant's convenience. Applicant's attention is also directed to the pertinent sections of the prior art.

83. Claims 5, 9, 10, 11, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller in view of IEEE 1164.

84. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller in view of Tzartzanis.

85. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tzartzanis.

86. As per Claim 5, Mueller teaches the limitations of Claim 1, as described above. However, Mueller does not expressly teach the limitation of Claim 5:

> 5. The method of claim 1, wherein providing an indication includes indicating when the released node is in an unknown logic state.

IEEE 1164 does teach (pp.2,4,5) that the node can be in an unknown state. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mueller with IEEE 1164 because doing so would increase the resolution of the simulation.

87. As per Claim 9, Mueller teaches the limitations of Claim 8, as described above. However, Mueller does not expressly teach the limitation of Claim 9:

> 9. The method of claim 8, wherein the initial node condition is forced again if the testing results in the node resolving to an unknown logic value.

IEEE 1164 does teach (pp.2,4,5) that the node can be in an unknown state. Moreover, the truth tables in IEEE 1164 show the results when an unknown signal and another signal are operated on by an AND or an OR gate. Moreover, IEEE 1164 teaches a "Forcing Unknown" state.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mueller with IEEE 1164 because doing so would reduce ambiguity in the simulation results.

88. As per Claim 10, Mueller teaches the limitations of Claims 8 and 9, as described above. However, Mueller does not expressly teach the limitation of Claim 10:

> 10. The method of claim 9, wherein the initial node condition is forced and simulation is repeated until the node resolves to a valid logic value.

IEEE 1164 does teach (pp.2,4,5) that the node can be in an unknown state. Moreover, the truth tables in IEEE 1164 show the results when an unknown signal and another signal are operated on by an AND or an OR gate. Moreover, IEEE 1164 teaches a "Forcing Unknown" state.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mueller with IEEE 1164 because doing so would reduce ambiguity in the simulation results.

89. As per Claim 11, Mueller teaches the limitations of Claims 8-10, as described above. However, Mueller does not expressly teach the limitation of Claim 11:

11. The method of claim 10, wherein monitoring only occurs after the node resolves to a valid logic value.

Mueller does teach (p.2, "Creating Signals") that the node can be in 5 different states, among them, the valid and invalid states. Moreover, Mueller teaches (p.3, "Delays and Constraints", "Miscellaneous") that timing diagrams can created to plot these signals. Thus the monitoring occurs both when the signal is valid and when it is invalid.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to monitor signals (plot them on a timing diagram) only when they are valid, because doing so would be a decrease in functionality from what is taught by Mueller and what is well known and commonly used in the art.

90. As per Claim 19, Mueller teaches the limitations of Claim 8, as described above. However, Mueller does not expressly teach the limitation of Claim 19:

19. The medium of claim 8, having further computer-executable instructions for indicating when the released node is in an unknown logic state.

IEEE 1164 does teach (pp.2,4,5) that the node can be in an unknown state.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mueller with IEEE 1164 because doing so would increase the resolution of the simulation.

91. In regards to the limitations of Claim 31:

31. An HDL simulated circuit device, comprising:
a first HDL module comprising:
a first input submodule inputting a first initial node condition;
a first conveyance submodule conveying the first initial node condition to a first simulated node;
a first monitor submodule monitoring the first simulated node for a first node condition; and
a first output submodule outputting a first indication when the first node condition is in an undesirable state;

a second HDL module comprising:
a second input submodule inputting a second initial node condition;
a second conveyance submodule conveying the second initial node condition to a second simulated node;
a release submodule releasing the node on a predetermined condition;
a second monitor submodule monitoring the second simulated node for a second node condition; and
a second output submodule outputting a second indication when the second node condition is in an undesirable state; and

wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

Mueller teaches inputting an initial node condition (p.2, "Creating Signals"), monitoring the node (p.3, "Miscellaneous"), and outputting indications when the node is in an undesirable state (p.3, "Miscellaneous).

However, Mueller does not expressly teach that his product is implemented in HDL. Moreover, Mueller does not expressly teach a first and second module, nor that the first module conveys the first initial node condition to the second input module.

Tzartzanis does teach implementing the above features in HDL. (pp.28-38, pp.65-70). Moreover, Tartanis teaches the use of modular blocks (pp.51-55).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the teachings of Mueller with Tzartzanis in order to implement the features in and HDL language such as Verilog, because this was well known and commonly used in the art.

Moreover, it would have been obvious to one of ordinary skill in the art to modify the teachings of Mueller with Tzartzanis in order to implement the features in a modular program, because this was well known and commonly used in the art.

92. In regards to the limitations of Claim 32:

32. An HDL simulated circuit device, comprising:
a first HDL module comprising:
a first input;
a first conveyance;
a first node condition output
a second HDL module comprising:
a second input;
a second conveyance;
a third HDL module comprising:
a release condition;
wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

Tzartzanis teaches the use of Verilog, an HDL language. Moreover, he teaches inputs (p.35, p.55), conveyance (p.37), outputs (pp.38-39), and release conditions (p.37). Moreover, Tzartzanis teaches Block statements and modules (pp.51-60).

However, Tzartzanis does not expressly teach three related modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make three related modules that perform these functions, because that is purely a matter of design choice.

Conclusion

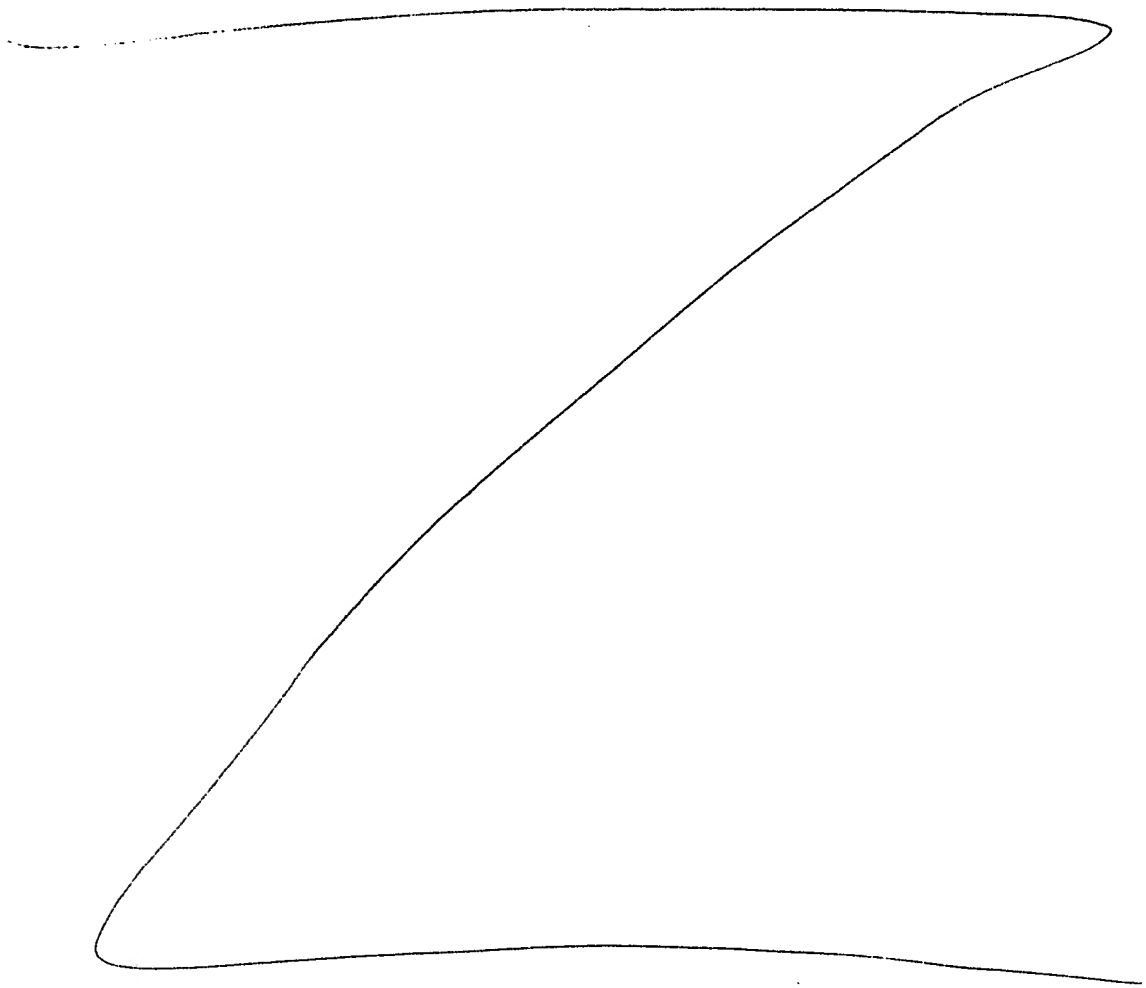
93. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

94. Silicon Integration Initiative, Inc. "Electronic Component Information eXchange (ECIX) – Timing Diagram Markup Language (TDML) Sample Instances". May 18, 1999.

This document has a screen shot of a Timing Diagram produced by the software program TimingDesigner. This screen shot shows that a Timing Diagram provides an indication when a signal is in a "pre-selected" condition.

The user can interpret this indication as an "error indication".

95. IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164). Copyright 1993. The IEEE Standard expressly teaches (pp.2,4,5) an "unknown state".



Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications:	(703) 746-7239
Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Patent Examiner

Art Unit 2123

April 26, 2002

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